IN THE CLAIMS:

Claims 1-15 (Canceled)

16. (Original) A fast pattern processor, comprising:

a data buffer that stores processing blocks associated with a protocol data unit (PDU);

a context memory subsystem associated with said data buffer that receives said processing blocks;

a pattern processing engine, associated with said context memory, that performs pattern matching upon said processing blocks; and

an output interface subsystem that receives said processing blocks from said data buffer or said context memory subsystem and re-transmits packets or payloads embodied within said processing blocks, said output interface subsystem, including:

a first-in-first-out (FIFO) buffer; and

an event edge synchronization system that provides a synchronous notification signal indicating that a block of data of said FIFO buffer has been retrieved and re-transmitted, said event edge synchronization system having:

a first clock zone device that generates an event signal based upon a first clock rate, said first clock zone device is associated with an output portion of said FIFO buffer;

a second clock zone device that receives said synchronous notification signal based upon a second clock rate and performs processing based upon said synchronous notification signal, said second clock rate asynchronous with said first clock rate; and

a synchronous notification subsystem that receives said event signal, synchronizes said event signal to said second clock rate based upon an edge transition of said event signal and said second clock rate, and generates said synchronous notification signal.

17. (Original) The fast pattern processor as recited in Claim 16 wherein said synchronous notification subsystem further includes:

a first logic device that generates a first intermediate signal based upon said event signal and a clock signal of said second clock zone device;

a second logic device that generates a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device;

a third logic device that generates a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and

a comparison logic device that generates said synchronous notification signal based upon said second and third intermediate signals.

18. (Original) The fast pattern processor as recited in Claim 17 wherein said first, second and third logic devices are "D" type flip-flops.

19. (Original) The fast pattern processor as recited in Claim 17 wherein said comparison logic device is an exclusive-OR (XOR) gate.

20. (Original) The fast pattern processor as recited in Claim 16 wherein said synchronous notification subsystem synchronizes said event signal to said second clock rate based upon a positive edge transition of said event signal.